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- ☐ **1. A fuzzy attributed graph approach to subcircuit ex  
problem**  
Nian Zhang; Wunsch, D.C., II;  
Fuzzy Systems, 2003. FUZZ '03. The 12th IEEE Interr  
Conference on  
Volume 2, 25-28 May 2003 Page(s):1063 - 1067 vol.2  
Digital Object Identifier 10.1109/FUZZ.2003.1206579  
Abstract | Full Text: PDF(364 KB) IEEE CNF
- ☐ **2. A circuit comparison system with rule-based funct  
isomorphism checking**  
Takashima, M.; Ikeuchi, A.; Kojima, S.; Tanaka, T.; Sa  
Sakata, J.;  
Design Automation Conference, 1988. Proceedings., 2  
ACM/IEEE  
12-15 June 1988 Page(s):512 - 516  
Digital Object Identifier 10.1109/DAC.1988.14808  
Abstract | Full Text: PDF(284 KB) IEEE CNF
- ☐ **3. Subislands: the probabilistic match assignment al  
subcircuit recognition**  
Rubanov, N.;  
Computer-Aided Design of Integrated Circuits and Sys  
Transactions on  
Volume 22, Issue 1, Jan. 2003 Page(s):26 - 38  
Digital Object Identifier 10.1109/TCAD.2002.805722  
Abstract | Full Text: PDF(724 KB) IEEE JNL
- ☐ **4. A logic-to-logic comparator for VLSI layout verifica**  
Maurer, P.M.; Schapira, A.D.;  
Computer-Aided Design of Integrated Circuits and Sys  
Transactions on  
Volume 7, Issue 8, Aug. 1988 Page(s):897 - 907  
Digital Object Identifier 10.1109/43.3221

Abstract | Full Text: PDF(968 KB) IEEE JNL

- ☐ **5. Constraints generation for analog circuits layout**  
Qinsheng Hao; Sheqin Dong; Song Chen; Xianlong Hong; Zhiyi Qu;  
Communications, Circuits and Systems, 2004. ICCCA: 2004 International Conference on  
Volume 2, 27-29 June 2004 Page(s):1339 - 1343 Vol.  
Abstract | Full Text: PDF(394 KB) IEEE CNF
- ☐ **6. Constraints generation for analog circuits layout**  
Qingsheng Hao; Song Chen; Xianlong Hong; Yi Su; Si Zhiyi Qu;  
Communications, Circuits and Systems, 2004. ICCCA: 2004 International Conference on  
Volume 2, 27-29 June 2004 Page(s):1334 - 1338 Vol.  
Abstract | Full Text: PDF(392 KB) IEEE CNF
- ☐ **7. An efficient subcircuit extraction algorithm by resource management**  
Zong Ling; Yun, D.Y.Y.;  
ASIC, 1996. 2nd International Conference on  
21-24 Oct. 1996 Page(s):9 - 14  
Digital Object Identifier 10.1109/ICASIC.1996.562738  
Abstract | Full Text: PDF(548 KB) IEEE CNF
- ☐ **8. A structural matching for two-dimensional visual pattern inspection**  
Koo, J.H.; Yoo, S.I.;  
Systems, Man, and Cybernetics, 1998. 1998 IEEE International Conference on  
Volume 5, 11-14 Oct. 1998 Page(s):4429 - 4434 vol.5  
Digital Object Identifier 10.1109/ICSMC.1998.727547  
Abstract | Full Text: PDF(936 KB) IEEE CNF
- ☐ **9. A Network Comparison Algorithm for Layout Verification of Integrated Circuits**  
Barke, E.;  
Computer-Aided Design of Integrated Circuits and Systems Transactions on  
Volume 3, Issue 2, April 1984 Page(s):135 - 141  
Abstract | Full Text: PDF(936 KB) IEEE JNL
- ☐ **10. Pattern search in hierarchical high-level designs**  
Terem, Z.; Kamhi, G.; Vardi, M.Y.; Iron, A.;  
Electronics, Circuits and Systems, 2004. ICECS 2004 Proceedings of the 2004 11th IEEE International Conference on  
13-15 Dec. 2004 Page(s):519 - 522  
Digital Object Identifier 10.1109/ICECS.2004.1399732  
Abstract | Full Text: PDF(525 KB) IEEE CNF
- ☐ **11. An improved layout verification algorithm (LAVA)**  
Abadir, M.S.; Ferguson, J.;  
Design Automation Conference, 1990. EDAC. Proceedings of the European  
12-15 March 1990 Page(s):391 - 395  
Digital Object Identifier 10.1109/EDAC.1990.136679  
Abstract | Full Text: PDF(508 KB) IEEE CNF

- ☐ **12. An efficient perfect algorithm for memory repair p**  
Hung-Yau Lin; Fu-Min Yeh; Ing-Yi Chen; Sy-Yen Kuo  
Defect and Fault Tolerance in VLSI Systems, 2004. D  
Proceedings. 19th IEEE International Symposium on  
10-13 Oct. 2004 Page(s):306 - 313  
Digital Object Identifier 10.1109/DFTVS.2004.134785  
Abstract | Full Text: PDF(705 KB) **IEEE CNF**



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